Refine Search

Search Results -

Terms	Documents
L2 same (((non adj1 volatile) or nonvolatile) adj1 memory)	30

Database:

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Search: L3

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DB=USPT,USOC; PLUR=YES; OP=OR		
L3 L2 same (((non adj1 volatile) or nonvolatile) adj1 memory)	30	L3
L2 ("universal serial bus" or USB) same host same computer	800	L2
L1 ("universal serial bus" or USB) same host same computer	748	L1

END OF SEARCH HISTORY

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Terms	Documents
L3	0

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L4	L3	0	L4
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	L2 same (((non adj1 volatile) or nonvolatile) adj1 memory)	30	L3
L2	("universal serial bus" or USB) same host same computer	800	L2
L1	("universal serial bus" or USB) same host same computer	748	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
(370/254 |370/419 |709/220 |709/221 |709/250 |709/226 |710/8 |710/9 |710/10 |710/33 |710/315 |710/63 |710/305 |710/100 |711/100 |711/104 |711/102 |711/147 |712/36 |714/23).ccls.	9030

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DB=USPT,USOC; PLUR=YES; OP=OR

L1   710/8-10,33,315,63,305,100;714/23;711/100,104,102,147;712/36;709/220,221,250,226;370/254,419.ccl

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L1 and L3	13

Database:

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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
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Search:

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side by
side

DB=USPT,USOC; PLUR=YES; OP=OR

L4   l1 and L3

L3   L2 same host same ((non adj1 volatile) or nonvolatile)

L2   ("universal serial bus" or USB) same memory

L1   710/8-10,33,315,63,305,100;714/23;711/100,104,102,147;712/36;709/220,221,250,226;370/254,419.ccl∕⌐

END OF SEARCH HISTORY

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- Active
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1	BRS	L1	12	("universal serial bus" or USB) same host same	USPAT	2004/07/26 09:55				0

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("universal serial bus" or USB) same host same microcomputer

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6727952 B1	20040427	7	Electronic device having common connector	348/372	348/207.1; 348/211.4;
2	☐	☐	US 6717477 B2	20040406	9	Circuit for controlling a non-conductive state of a	331/46	710/8
3	☐	☐	US 6625738 B1	20030923	11	USB apparatus that turns on computer power supply using	713/310	710/67
4	☐	☐	US 6615192 B1	20030902	23	Contents copying system, copying method,	705/57	705/1; 705/50;
5	☐	☐	US 6577337 B1	20030610	14	Display apparatus for visual communication	348/207.1	348/14.08; 348/211.3;
6	☐	☐	US 6287198 B1	20010911	12	Optical gun for use with computer games	463/37	463/36; 463/38;
7	☐	☐	US 6279053 B1	20010821	11	Apparatus for transmitting key-in data and video data	710/30	710/5; 710/67
8	☐	☐	US 6230277 B1	20010508	13	Peripheral device for reducing power supplied from	713/320	713/310; 713/322;
9	☐	☐	US 6219736 B1	20010417	26	Universal serial bus (USB) RAM architecture for use	710/315	370/259; 370/420;
10	☐	☐	US 6067589 A	20000523	18	USB legacy support system	710/63	710/15; 710/315;
11	☐	☐	US 6049880 A	20000411	13	Computer display monitor apparatus and method for	713/300	323/278; 323/286;

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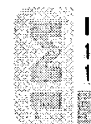**No documents matched your query.**

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Results Key:
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1 **TKDM - a reconfigurable co-processor in a PC's memory slot**
Plessl, C.; Platzner, M.;
Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE Interna
Conference on , 15-17 Dec. 2003
Pages:252 - 259

[Abstract]   [PDF Full-Text (532 KB)]   **IEEE CNF**

2 **Balancing the 3D pipeline in the mainstream PC**
Eggebrecht, L.C.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Pages:300 - 306

[Abstract]   [PDF Full-Text (452 KB)]   **IEEE CNF**

3 **The Mpact media processor redefines the multimedia PC**
Foley, P.;
Compcon '96. 'Technologies for the Information Superhighway' Digest of
Papers , 25-28 Feb. 1996
Pages:311 - 318

[Abstract]   [PDF Full-Text (676 KB)]   **IEEE CNF**

4 **An organization and interface for sensor-driven semiconductor proc
control systems**
Najafi, N.; Wise, K.D.;
Semiconductor Manufacturing, IEEE Transactions on , Volume: 3 , Issue: 4 , |
1990
Pages:230 - 238

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[Abstract]   [PDF Full-Text (888 KB)]   **IEEE JNL**

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5 **Intelligent and free user configurable low cost data acquisition unit**
Edelmoser, K.; Anselmi, C.;
Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of th
1996 IEEE IECON 22nd International Conference on , Volume: 2 , 5-10 Aug.
Pages:1301 - 1305 vol.2

[Abstract]   [PDF Full-Text (320 KB)]   **IEEE CNF**

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6 **A hybrid real-time UNIX controller for the Donner 600-crystal positi tomograph**
Huesman, R.H.; Klein, G.J.; Fleming, T.K.;
Nuclear Science Symposium and Medical Imaging Conference, 1994., 1994 IE
Conference Record , Volume: 4 , 30 Oct.-5 Nov. 1994
Pages:1648 - 1651 vol.4

[Abstract]   [PDF Full-Text (288 KB)]   **IEEE CNF**

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L3: Entry 1 of 30   File: USPT   Jun 29, 2004

DOCUMENT-IDENTIFIER: US 6757783 B2
TITLE: Portable storage medium based on universal serial bus standard and UFI
standard

Brief Summary Text (12):
Reference numeral 20 designates the USB flash drive containing a nonvolatile memory
that is connected with the USB port 11 of the host computer 10 to store data
transmitted from the host computer 10, and write, read and delete data through the
host computer 10. Reference numeral 21 denotes a USB connector connected with the
USB port 11 of the host computer 10 physically, and 22 represents a memory for
storing data sent from the host computer 10, which includes at least one flash
memory 221.about.22n that is a nonvolatile memory. The flash memory 221.about.22n
has two kinds of NOR and NAND types. The USB flash drive 20 employs the cheap NAND
type flash memory.

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L3: Entry 1 of 30   File: USPT   Jun 29, 2004

US-PAT-NO: 6757783
DOCUMENT-IDENTIFIER: US 6757783 B2

TITLE: Portable storage medium based on universal serial bus standard and UFI standard

DATE-ISSUED: June 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Koh; Young Sook	Seoul			KR

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Daesung EC&P Co., Ltd.	Seoul			KR	03

APPL-NO: 09/ 996219   [PALM]
DATE FILED: November 28, 2001

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
KR	2001-70564	November 13, 2001

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/115; 711/159, 711/169, 710/105, 710/313
US-CL-CURRENT: 711/115; 710/105, 710/313, 711/159, 711/169

FIELD-OF-SEARCH: 711/103, 711/115, 711/137, 711/140, 711/107, 711/169, 711/133, 711/134, 711/141, 711/142, 711/143, 711/146, 711/154, 711/159, 710/105, 710/106, 710/313, 710/315

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5937427	August 1999	Shinagawa et al.	711/113
☐	6012103	January 2000	Sartore	710/8
☐	6088755	July 2000	Kobayashi et al.	710/129
	6148354	November 2000	Ban	710/102

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☐   6275911   August 2001   Terada et al.   711/154

☐   6401163   June 2002   Kondo et al.   711/100

☐   6442668   August 2002   Sudo   711/211

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
10-2001-0020441	March 2001	KR	
2001-0035042	May 2001	KR	
2001-0036746	May 2001	KR	
2001-0071332	July 2001	KR	
2001-0095475	November 2001	KR	
2002-0041221	June 2002	KR	

OTHER PUBLICATIONS

"Universal Serial Bus Mass Storage Class Specification Overview", .COPYRGT. 1998
USB Implementers Forum, p. 1-8.*
"Universal Serial Bus Mass Storage Class UFI Command Specification", .COPYRGT. 1998
USB Implementers Forum, p. 1-53.

ART-UNIT: 2187

PRIMARY-EXAMINER: Sparks; Donald

ASSISTANT-EXAMINER: Peugh; Brian R.

ATTY-AGENT-FIRM: Lilling & Lilling P.C.

ABSTRACT:

There is provided a portable storage medium, based on USB standard, connected to a
USB port of a host computer applying UFI protocol. The portable storage medium
comprises a USB connector through which the storage medium is physically connected
to the USB port of the host computer; at least one nonvolatile flash memory for
storing data transmitted from the host computer; a program storage for storing a
predetermined operation program based on USB and UFI; and a controller for
controlling the entire operation of the storage medium based on the operation
program stored in the program storage. The operation program of the program storage
includes a memory processing block for checking and updating header block
information of the flash memory, a device recognition processing block for
transmitting device descriptor information and interface descriptor information for
loading a UFI driver to the host computer, and a UFI processing block for
generating predetermined UFI response packets by UFI commands sent from the host
computer to transmit them to the host computer.

10 Claims, 14 Drawing figures

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L3: Entry 29 of 30   File: USPT   Sep 28, 1999

DOCUMENT-IDENTIFIER: US 5958020 A
TITLE: Real time event determination in a universal serial bus system

Detailed Description Text (7):
FIG. 1 shows a block diagram of computer system 122 utilizing a USB architecture in
accordance with the present invention. In general, computer system 122 used by an
embodiment of the present invention comprises an address/data bus 100 for
communicating information, one or more host processors 102 coupled with bus 100 for
processing information and instructions, a computer readable volatile memory unit
106 (e.g. random access memory unit, static RAM, dynamic RAM, etc.) coupled with
bus 100 for storing information and instructions for the host processor 102, a
computer readable non-volatile memory unit 104 (e.g., read only memory unit,
programmable ROM, flash memory, EPROM, EEPROM, etc.) coupled with bus 100 for
storing static information and instructions for the host processor 102, a computer
readable data storage device 108 such as a magnetic or optical disk and disk drive
(e.g., hard drive or floppy diskette) coupled with bus 100 for storing information
and instructions, a USB controller 110 coupled to bus 100 to provide an interface
to control all the peripheral devices connected to root hub 111, and a root hub 111
coupled to USB controller 110 to provide connection ports to couple peripheral
devices to computer system 122.

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L3: Entry 29 of 30   File: USPT   Sep 28, 1999

US-PAT-NO: 5958020
DOCUMENT-IDENTIFIER: US 5958020 A

TITLE: Real time event determination in a universal serial bus system

DATE-ISSUED: September 28, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Evoy; David R.	Tempe	AZ		
Goff; Lonnie	Tempe	AZ		
Chambers; Peter	Phoenix	AZ		
Eidson; Mark	Tempe	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
VLSI Technology, Inc.	San Jose	CA			02

APPL-NO: 08/ 960483   [PALM]
DATE FILED: October 29, 1997

INT-CL: [06] G06 F 13/14, G06 F 13/20

US-CL-ISSUED: 710/3; 710/15, 710/30, 710/46, 710/63
US-CL-CURRENT: 710/3; 710/15, 710/30, 710/46, 710/63

FIELD-OF-SEARCH: 710/1, 710/3, 710/15, 710/18, 710/30, 710/46, 710/47, 710/63

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5535251	July 1996	Sugawara	375/356
☐	5717762	February 1998	Aihara et al.	380/49
☐	5812625	September 1998	Potier et al.	377/20
☐	5890015	March 1999	Garney et al.	395/882

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ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Perveen; Rehana

ATTY-AGENT-FIRM: Wagner, Murabito & Hao

ABSTRACT:

The system of the present invention comprises a system for implementing a real time
capability in peripheral devices. The system of the present invention functions
with a computer system including a processor, a memory, and a video controller,
each coupled to a system bus. A USB (universal serial bus) controller is also
coupled to the system bus for interfacing peripheral devices on a USB cable to the
computer system. A first and second register are included in the USB controller for
storing a controller frame number and a controller frame remaining, and a second
and third register are included in the peripheral device for storing a device frame
number and a device frame remaining. The peripheral device is coupled to the USB
controller via a USB cable. A screen reference register is coupled to receive the
controller frame number and the controller frame remaining from the USB controller
and is coupled to receive a reference signal from a video controller. In response
to receiving the reference signal, the screen reference register stores the
controller frame number and the controller frame remaining. The peripheral device
transmits the device frame number and the device frame remaining to the computer
system in response to the occurrence of an event. The controller frame remaining
and the controller frame number are subsequently compared with the device frame
remaining and the device frame number to determine a computer system time (e.g., a
real time) of the occurrence of the event.

19 Claims, 7 Drawing figures

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L3: Entry 26 of 30   File: USPT   Jan 4, 2000

DOCUMENT-IDENTIFIER: US 6012103 A
TITLE: Bus interface system and method

Detailed Description Text (3):
FIG. 1 is a diagram illustrating a standardized bus interface, such as a
conventional computer system 20, that may include a host computer system 22 and a
peripheral device 24. The peripheral device is connected to the host computer by a
universal serial bus (USB) 26. The host computer may include a central processing
unit (CPU) 28 connected to a USB interface (I/F) circuit 30, and the USB standard
provides a universal electrical and physical interface for the peripheral devices
via bus 26. The CPU executes software application code located in a memory 31 and
communicates data to and from the peripheral device through the USB interface and
the USB 26. The host computer may also include an operating system 32 which may
include a software device driver 33. The peripheral device 24 may include a USB
interface circuit 34, a CPU 36 and a non-volatile memory 38 that may store
configuration information describing the characteristics of the peripheral device.
The non-volatile memory may be a read only memory (ROM) or an erasable programmable
read only memory (EPROM).

Detailed Description Text (4):
When the peripheral device is initially connected to the USB, an enumeration
process is conducted in which the host computer determines the characteristics of
the peripheral device by receiving the configuration information from the memory 38
within the peripheral device, and configures the USB according to the
characteristics of the peripheral device. As shown, the configuration information
about the characteristics of the peripheral device in a conventional USB system is
stored in a non-volatile memory 38 on the peripheral device. The data about the
characteristics of the peripheral device is programmed into the non-volatile memory
at the factory, and the characteristics of the peripheral device may not be easily
altered. In addition, the memory in the peripheral device stores all of the
configuration information about the peripheral device which may require a large
amount of memory in the peripheral device.

Detailed Description Text (6):
FIG. 2 is a diagram illustrating a computer system 50 that may have a universal
serial bus system in accordance with the invention. The computer system may include
a host computer 52 connected to a peripheral device 54 by a universal serial bus
(USB) 60. The host computer may include a CPU 62, a memory 64, an operating system
65 and a USB interface circuit 66. One or more peripheral device drivers, such as a
first peripheral device driver 68, may be stored in the operating system 65. Each
device driver contains information about the proper configuration of the USB for a
particular class of peripheral devices. The operating system within the host
computer may also contain a plurality of different configuration information sets
70, which may include configuration data for a particular peripheral device
(including which device driver to use), microprocessor code to be executed by a CPU
located in the peripheral device, or logic configuration data to configure logic
circuits in the peripheral device. This invention advantageously enables these
configuration information sets to be updated or altered easily since they are
located in the host computer and not in a non-volatile memory in the peripheral
device.

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Detailed Description Text (16):
As shown in FIG. 5, peripheral device "A" 144 may have a unique manufacturer
signature in the non-volatile memory 178. When the peripheral device is connected
to the computer system, the enumeration process begins in which the USB interface
system 170 is recognized by the USB as a generic device and the unique manufacturer
signature is read from the non-volatile memory by the CPU 150 over the USB 149. The
unique signature identifies device "A" characteristics 164 as the appropriate
configuration information and that configuration information may be downloaded over
the USB 149 into the memory 174 of the peripheral device as shown by dashed arrow
180. Then the electrical simulation of the disconnection and reconnection of the
peripheral device occurs, as described above, which cause re-enumeration of the
peripheral device. During re-enumeration, device driver "A" 158, which is
identified by device "A" characteristics 164 as the appropriate device driver, is
loaded from the operating system into the memory, as shown by arrow 182, such that
the peripheral device is now recognized as a peripheral device with device "A"
characteristics. Thus, a generic hardware USB interface system may be incorporated
into a peripheral device and the particular characteristics for the particular
peripheral device may be later downloaded from the host computer into the
peripheral device.

Detailed Description Text (17):
Similarly, as shown in FIGS. 6 and 7, the peripheral devices 146, 148 may include
the generic USB interface system and a unique manufacturer signature in the non-
volatile memory and may be re-enumerated in accordance with the invention so that
the appropriate device characteristics are downloaded from the host computer over
the USB into the memory of the peripheral device and the appropriate device driver
may be selected by the host computer. Thus, peripheral device "B" 146 (shown in
FIG. 6) may have device "B" characteristics 166 downloaded into its memory, as
shown by dashed arrow 184 in FIG. 6, and the host computer may use device driver
"B" 160, as shown by arrow 186 in FIG. 6. The peripheral device "C" 148 (shown in
FIG. 7) may have device "C" characteristics 168 downloaded into its memory as shown
by the dashed arrow 188 in FIG. 7 and the host computer may use device driver "C"
162 as shown by arrow 190 in FIG. 7. Thus, a generic USB interface system may be
incorporated into a plurality of different peripheral devices, the appropriate
configuration information may be downloaded into the peripheral device, and the re-
enumeration recognizes the peripheral device as a manufacturer specific device. The
re-enumeration of the generic peripheral device ensures that the host computer
discards all device driver information about the generic connection and loads the
manufacturer-specific device driver software.

h   e b   b cg b   cc   e

☐ | Generate Collection | | Print |

L3: Entry 26 of 30   File: USPT   Jan 4, 2000

US-PAT-NO: 6012103
DOCUMENT-IDENTIFIER: US 6012103 A

TITLE: Bus interface system and method

DATE-ISSUED: January 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sartore; Ronald H.	San Diego	CA		
Larky; Steven P.	Del Mar	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Cypress Semiconductor Corp.	San Jose	CA			02

APPL-NO: 08/ 886923   [PALM]
DATE FILED: July 2, 1997

INT-CL: [06] G06 F 13/368

US-CL-ISSUED: 710/8; 710/9, 710/10
US-CL-CURRENT: 710/8; 710/10, 710/9

FIELD-OF-SEARCH: 379/395, 709/220, 709/250, 711/114, 711/115, 711/130, 713/100, 710/9

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

| Search Selected | | Search ALL | | Clear |

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4641261	February 1987	Dwyer et al.	
☐	4862355	August 1989	Newman et al.	
☐	5289580	February 1994	Latif et al.	
☐	5428748	June 1995	Davidson et al.	710/9
☐	5488657	January 1996	Lynn et al.	379/395
☐	5574859	November 1996	Yeh	
☐	5577213	November 1996	Avery et al.	

h   e b   b g e e e f   c   e   b   e   ge

☐	5586268	December 1996	Chen et al.	
☐	5606672	February 1997	Wade	
☐	5615344	March 1997	Corder	
☐	5634074	May 1997	Devon et al.	395/828
☐	5671355	September 1997	Collins	709/250
☐	5687346	November 1997	Shinohara	711/130
☐	5701429	December 1997	Legvold et al.	711/114
☐	5794033	August 1998	Aldebert et al.	713/100
☐	5802558	September 1998	Pierce	711/115
☐	5838907	November 1998	Hansen	709/220

ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Yuan; Chien

ATTY-AGENT-FIRM: Maiorana, P.C.; Christopher P.

ABSTRACT:

A system and method for reconfiguring a peripheral device connected by a computer bus and port to a host from a first generic configuration to a second manufacturer specific configuration is provided in which the configuration of a peripheral device may be electronically reset. A peripheral interface device for a standardized computer peripheral device bus and port is also provided in which a physical disconnection and reconnection of the peripheral device is emulated to reconfigure the bus and port for a particular peripheral device.

33 Claims, 8 Drawing figures

h   e b   b g e e e f   c   e   b'   e ge

☐ Generate Collection | Print |

L3: Entry 19 of 30   File: USPT   Nov 19, 2002

DOCUMENT-IDENTIFIER: US 6484219 B1
** See image for Certificate of Correction **
TITLE: Host-specified USB device requests

Detailed Description Text (5):
USB peripheral device 12 also has one or more processors 30 and one or more forms
of computer-readable memory media 31, including at least some form of non-volatile
memory media 32. Various USB-related information is stored in the non-volatile
memory, such as descriptors 33 that are provided to host 11 upon request. Operating
logic in the form of a sequentially-executed program 34 is stored in the memory,
from where it is executed by processor 30.

h   e b   b cg b   cc   e

L3: Entry 19 of 30   File: USPT   Nov 19, 2002

US-PAT-NO: 6484219
DOCUMENT-IDENTIFIER: US 6484219 B1
** See image for Certificate of Correction **

TITLE: Host-specified USB device requests

DATE-ISSUED: November 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dunn; John C.	Issaquah	WA		
Ray; Kenneth D.	Redmond	WA		
Bhesania; Firdosh K.	Kirkland	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Microsoft Corporation	Redmond	WA			02

APPL-NO: 09/ 498056   [PALM]
DATE FILED: February 4, 2000

INT-CL: [07] G06 F 13/42

US-CL-ISSUED: 710/42; 710/11, 710/313
US-CL-CURRENT: 710/42; 710/11, 710/313

FIELD-OF-SEARCH: 710/2-5, 710/8-11, 710/72-74, 710/62-63, 710/305-315

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

| Search Selected | Search ALL | Clear |

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
□	5835791	November 1998	Goff et al.	710/62
□	6219736	April 2001	Klingman	710/129
□	6233640	May 2001	Luke et al.	710/129
□	6256687	July 2001	Ellis et al.	710/71
□	6260084	July 2001	Wilson et al.	710/38
□	6343260	January 2002	Chew	702/122

☐ <u>6389495</u>   May 2002   Larky et al.   710/129
☐ <u>6389560</u>   May 2002   Chew   714/43

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
00/59594	October 2000	WO	
0157679	August 2001	WO	

OTHER PUBLICATIONS

"USB Device Framework", Revision 1.1, Chapter 9, Universal Serial Bus
Specification, Sep. 1998.
"Universal Serial Bus Common Class Specification", SystemSoft Corporation, Intel
Corporation, Dec. 1997.

ART-UNIT: 2182

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Lee & Hayes, PLLC

ABSTRACT:

A USB device is configured to support a non-USB-defined device request that is
specific to an application program or operating system. The device request is
supported by using a device-specific or vendor-specific request code, which is
allowed to vary from device to device. To determine the proper request code, the
host performs a GET_DESCRIPTOR device request, specifying a predetermined string
descriptor. The requested string descriptor designates the request code to be used
in the non-USB-defined device request.

28 Claims, 3 Drawing figures

h   e b   b g e e e f   c   e   b   e ge

```
US-PAT-NO:              6717477

DOCUMENT-IDENTIFIER:    US 6717477 B2

TITLE:                  Circuit for controlling a non-conductive state of a USB
                        interface
```

---------- KWIC ---------

Abstract Text - ABTX (1):
   There are provided an output terminal P1 to be also used as a terminal to
which a USB signal line is connected, a power-on reset circuit 80 for
generating a reset signal RES in response to power supply from the USB signal
line, and an RC oscillator 81 for starting oscillation immediately in response
to the reset signal RES. The output of the RC oscillator 81 is used for a
system clock to operate a microcomputer and to set the level of the output
terminal P1. Consequently, USB signal lines 110 and 111 are forcibly set to a
level in a non-connection state for a period before a USB interface circuit 30
can respond to a bus reset signal sent from a host.

Brief Summary Text - BSTX (3):
   The present invention relates to a microcomputer comprising a USB interface
circuit for interfacing data transmission and receipt between a host and the
microcomputer through a USB signal line.

Brief Summary Text - BSTX (14):
   It is an object of the invention to provide a microcomputer comprising a USB
interface capable of reliably receiving communication data also in the case in
which a personal computer to be a host knows that the microcomputer is
connected to a USB cable and transmits the communication data immediately after
the issuance of a bus reset signal.

Brief Summary Text - BSTX (15):
   The invention provides a microcomputer comprising a USB interface circuit
for interfacing transmission and receipt of data between a host and the
microcomputer through a USB signal line, comprising state setting means for

US006717477B2

(12) **United States Patent**
Kondo

(10) Patent No.: **US 6,717,477 B2**
(45) Date of Patent: **Apr. 6, 2004**

(54) **CIRCUIT FOR CONTROLLING A NON-CONDUCTIVE STATE OF A USB INTERFACE**

(75) Inventor: Hideo Kondo, Oaama (JP)

(73) Assignee: Sanyo Electric Co., Ltd., Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/010,348

(22) Filed: Nov. 8, 2001

(65) **Prior Publication Data**

US 2002/0057134 A1 May 16, 2002

(30) **Foreign Application Priority Data**

Nov. 10, 2000 (JP) P2000-342845

(51) Int. Cl.^{7} H03B 5/20
(52) U.S. Cl. 331/46; 710/8
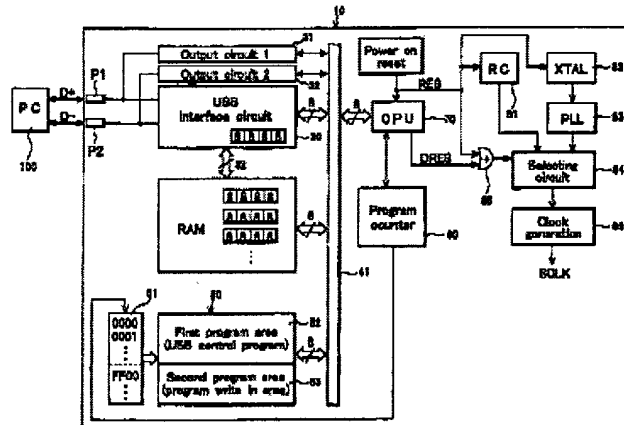(58) Field of Search .... 331/46, 49, 1 A, 331/17; 713/1, 2; 710/5, 10, 12, 63, 315

(56) **References Cited**

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6,178,513 B1 * 1/2001 Lee 713/300

6,205,502 B1 * 3/2001 Endo et al. 710/100
6,351,809 B1 * 2/2002 St. Pierre et al. 713/1
6,370,603 B1 * 4/2002 Silverman et al. 710/72

FOREIGN PATENT DOCUMENTS

WO   WO 98/27482   6/1998

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Korean Office Action dated May 29, 2003.

* cited by examiner

Primary Examiner—Robert Pascal
Assistant Examiner—Joseph Chang
(74) Attorney, Agent, or Firm—Fish & Richardson P.C.

(57)   **ABSTRACT**

There are provided an output terminal P1 to be also used as a terminal to which a USB signal line is connected, a power-on reset circuit 80 for generating a reset signal RES in response to power supply from the USB signal line, and an RC oscillator 81 for starting oscillation immediately in response to the reset signal RES. The output of the RC oscillator 81 is used for a system clock to operate a micro-computer and to set the level of the output terminal P1. Consequently, USB signal lines 110 and 111 are forcibly set to a level in a non-connection state for a period before a USB interface circuit 30 can respond to a bus reset signal sent from a host.

11 Claims, 4 Drawing Sheets

File   Edit   View   Tools   Window   Help

US-PAT-NO: 6219736

DOCUMENT-IDENTIFIER: US 6219736 B1

TITLE: Universal serial bus (USB) RAM architecture for use with
                         microcomputers via an interface optimized for integrated
                         services device network (ISDN)

---------- KWIC ---------

▮
Brief Summary Text - BSTX (3):
    This invention relates generally to the field of general purpose
microcomputers and particularly to a microcomputer unit including a serial
interface controller such as the Universal Serial Bus (USB) RAM device to
facilitate communication between a host and a microcontroller.

Detailed Description Text - DETX (68):
    The receipt of a token for a specific endpoint always initiates a new
transaction, and causes the virtual endpoint register in the virtual endpoint
register file storage location 248 that is associated with the specific
endpoint to be partially loaded into the corresponding endpoint register file
198 thereby pre-configuring the USB RAM device 130 for the transaction. Some
transactions are periodic, or in some way predictable, and the pre-configured
endpoint registers generally are capable of immediate service in these cases.
For example, the ISO IN registers (shown in the third row, or row `2`, of the
endpoint register file 198) can be preset to point to the data buffer 254 that
in FIG. 5 will periodically be sent to the USB host. Some transactions are a
periodic and asynchronous, and cannot generally be anticipated, an example of
such types of transactions are SETUP transactions on the CONTROL pipe that
issue standard request packets to the microcontroller device 140. In most
cases the microcontroller device 140 cannot retrieve the request and setup the
response thereto in the allowed response time. Therefore, the USB RAM device
130 initiates "auto-NAK" transactions. That is, when the microcontroller
device is not prepared to respond to a request from the host, the USB RAM
device upon detection thereof, automatically responds to the host with a "NAK"
token thereby informing the host that the microcomputer is not ready, which
implies that the host must try again later. "NAK" tokens are repeatedly and
indefinitely sent to the host by the USB RAM device until such time as when the

US006219736B1

(12) **United States Patent** (10) Patent No.: **US 6,219,736 B1**
Klingman (45) Date of Patent: Apr. 17, 2001

(54) **UNIVERSAL SERIAL BUS (USB) RAM ARCHITECTURE FOR USE WITH MICROCOMPUTERS VIA AN INTERFACE OPTIMIZED FOR INTEGRATED SERVICES DEVICE NETWORK (ISDN)**

(76) Inventor: Edwin E. Klingman, 3000 Hwy. 84, San Gregorio, CA (US) 94074

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/191,443

(22) Filed: Nov. 12, 1998

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/846,118, filed on Apr. 24, 1997, now Pat. No. 5,660,001.

(51) Int. Cl.[7] G06F 13/00
(52) U.S. Cl. 710/129; 710/14; 710/52;
710/100; 710/128; 709/226; 709/250; 370/259;
370/420; 370/524
(58) Field of Search 710/52, 14, 100,
710/128, 129; 709/250, 226; 370/259, 420,
524

(56) **References Cited**

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4,634,583 5/1986 Ross et al. 710/100
4,799,156 1/1989 Shavit et al. 705/26

(List continued on next page.)

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Don Jokmen, "Universal Serial Bus System Architecture".

Primary Examiner—Thomas C. Lee
Assistant Examiner—Tammara Peyton

(74) Attorney, Agent, or Firm—Oppenheimer, Wolff & Donnelly, LLP; Claude A. S. Hamrick

(57) **ABSTRACT**

A RAM-based interrupt-driven interface device is disclosed for establishing a communication link between a universal serial bus (USB) host and a microcontroller device for providing a control function, the interface device being operative to receive digital information in the form of command, data and control packets from the host and to process the packets and communicate the processed digital information to the microcontroller device, and in response thereto, the microcontroller device being operative to communicate digital information to the interface device for processing and transfer thereof to the host. The interface device includes means for receiving a command generated by the host through a USB bus, means for storing the host-generated command and for generating an interface device interrupt signal upon storage of said host-generated command for use by the microcontroller device in responding to the host-generated command, a microcontroller bus for transferring microcontroller information and the interface device interrupt signal between the interface device and the microcontroller device. The interface device further includes means for receiving a microcontroller command from the microcontroller device in response to said interface device interrupt signal and means for storing the microcontroller command and it is operative to generate a microcontroller device interrupt signal upon storage of the microcontroller command for use by the interface device in developing an address for identification of the interface device to the host during subsequent communications therebetween, wherein during communication between the host and the interface device, the interface device-developed address is used by the interface device to identify host-provided information in the form of packets, and upon processing of the host-provided information, to provide the microcontroller device with the necessary information to allow it to respond to the host thereby allowing a generic microcontroller device to be flexibly interfaced with a USB host for communication therebetween.

35 Claims, 10 Drawing Sheets
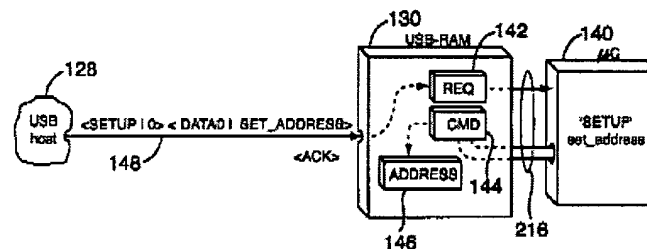
US006044428A

United States Patent [19]

Rayabhari

[11]   Patent Number: 6,044,428

[45]   Date of Patent: Mar. 28, 2000

[54]   CONFIGURABLE UNIVERSAL SERIAL BUS NODE

[75]   Inventor: Madhu Rayabhari, Cupertino, Calif.

[73]   Assignee: Fairchild Semiconductor Corporation, South Portland, Me.

[21]   Appl. No.: 09/040,110

[22]   Filed: Mar. 17, 1998

[51]   Int. Cl.⁷ G06F 13/10; G06F 13/40; G06F 15/17; G06F 3/00

[52]   U.S. Cl. 710/129; 710/63; 710/64

[58]   Field of Search 710/100, 101, 710/104, 63, 64, 72, 126, 129, 3, 128; 712/37; 345/156, 168; 709/231; 370/257, 364, 912; 455/6.3

[56]   References Cited

                 U.S. PATENT DOCUMENTS

5,396,639   3/1995   Suzuga et al. 712/37

|			
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5,623,586	4/1997	Hall et al.	712/32
5,659,801	8/1997	Kopsaftis	710/62
5,784,581	7/1998	Hannah	710/110
5,818,948	10/1998	Gulick	381/77
5,841,424	11/1998	Kikinis	345/168
5,859,993	1/1999	Snyder	712/208
5,914,677	6/1999	Gulick	364/400.01

Primary Examiner—Gopal C. Ray
Attorney, Agent, or Firm—Mikio Ishimaru

[57]   ABSTRACT

A Universal Serial Bus node having a non-volatile memory is preprogrammed with the data bits necessary to configure an attached state machine to become a translator or modified translator for signals from a computer peripheral device. On startup, the Universal Serial Bus node is configured to translate signals to and from the computer peripheral device into USB protocol signals to and from a Universal Serial Bus equipped computer in order to assure proper communication therebetween.

26 Claims, 1 Drawing Sheet
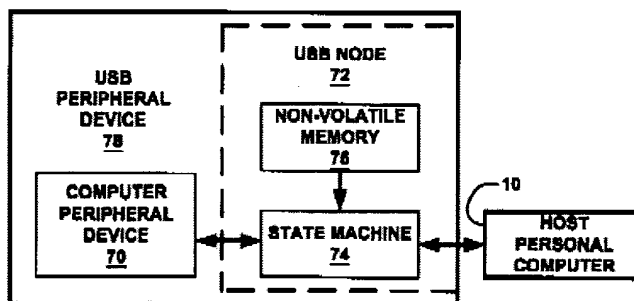
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US-PAT-NO:              6044428

DOCUMENT-IDENTIFIER:   US 6044428 A
**See image for Certificate of Correction**

TITLE:                 Configurable universal serial bus node


---------- KWIC ---------


Brief Summary Text - BSTX (8):
   The problem with the USB is that every computer peripheral device must have
a microcomputer, microprocessor or microcontroller (hereinafter generically
referred to as "microcomputer") capable of responding to the queries from the
host PC.  The microcomputer has to have USB logic attached to it, memory
associated with it, and the ability to handle communication with the host PC
with software which monitors the signals almost at a bit and byte level.
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Hit List

Search Results - Record(s) 1 through 10 of 13 returned.

☐ 1.   Document ID: US 6601109 B1

Using default format because multiple data bases are involved.

L4: Entry 1 of 13   File: USPT   Jul 29, 2003

US-PAT-NO: 6601109
DOCUMENT-IDENTIFIER: US 6601109 B1

TITLE: USB-based networking and I/O hub

DATE-ISSUED: July 29, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bealkowski; Richard	Redmond	WA		
Bland; Patrick M.	Raleigh	NC		

US-CL-CURRENT: <u>709/250</u>; <u>709/238</u>, <u>709/245</u>, <u>710/105</u>, <u>710/313</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De |

☐ 2.   Document ID: US 6594717 B2

L4: Entry 2 of 13   File: USPT   Jul 15, 2003

US-PAT-NO: 6594717
DOCUMENT-IDENTIFIER: US 6594717 B2

TITLE: Apparatus and method for dedicated interconnection over a shared external
bus

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De |

☐ 3.   Document ID: US 6502146 B1

L4: Entry 3 of 13   File: USPT   Dec 31, 2002

US-PAT-NO: 6502146
DOCUMENT-IDENTIFIER: US 6502146 B1

TITLE: Apparatus and method for dedicated interconnection over a shared external
bus

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`| Full | Title | Citation | Front | Review | Classification | Date | Reference | ████████ | ████████ | Claims | KWIC | Draw De`

☐ 4.   Document ID: US 6493770 B1

L4: Entry 4 of 13   File: USPT   Dec 10, 2002

US-PAT-NO: 6493770
DOCUMENT-IDENTIFIER: US 6493770 B1

TITLE: System for reconfiguring a peripheral device by downloading information from a host and electronically simulating a physical disconnection and reconnection to reconfigure the device

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | ████████ | ████████ | Claims | KWIC | Draw De`

☐ 5.   Document ID: US 6466994 B1

L4: Entry 5 of 13   File: USPT   Oct 15, 2002

US-PAT-NO: 6466994
DOCUMENT-IDENTIFIER: US 6466994 B1

TITLE: Method and system for programming a system board using a peripheral controller

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | ████████ | ████████ | Claims | KWIC | Draw De`

☐ 6.   Document ID: US 6308227 B1

L4: Entry 6 of 13   File: USPT   Oct 23, 2001

US-PAT-NO: 6308227
DOCUMENT-IDENTIFIER: US 6308227 B1

TITLE: System for detecting a wireless peripheral device by a host computer transmitting a hail message including a persistent host identifier and a host address generated

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | ████████ | ████████ | Claims | KWIC | Draw De`

☐ 7.   Document ID: US 6263392 B1

L4: Entry 7 of 13   File: USPT   Jul 17, 2001

US-PAT-NO: 6263392
DOCUMENT-IDENTIFIER: US 6263392 B1

TITLE: Method and apparatus for interfacing multiple peripheral devices to a host computer

h   e b   b g e e f   e c   ef   b   e

`Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De`

☐ 8. Document ID: US 6249825 B1

L4: Entry 8 of 13   File: USPT   Jun 19, 2001

US-PAT-NO: 6249825
DOCUMENT-IDENTIFIER: US 6249825 B1

TITLE: Universal serial bus interface system and method

`Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De`

☐ 9. Document ID: US 6226701 B1

L4: Entry 9 of 13   File: USPT   May 1, 2001

US-PAT-NO: 6226701
DOCUMENT-IDENTIFIER: US 6226701 B1
** See image for **Certificate of Correction** **

TITLE: Method and system for accurate temporal determination of real-time events
within a universal serial bus system

`Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De`

☐ 10. Document ID: US 6044428 A

L4: Entry 10 of 13   File: USPT   Mar 28, 2000

US-PAT-NO: 6044428
DOCUMENT-IDENTIFIER: US 6044428 A
** See image for **Certificate of Correction** **

TITLE: Configurable universal serial bus node

`Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De`

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Terms	Documents
L1 and L3	13

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      L4: Entry 10 of 13   File: USPT   Mar 28, 2000

US-PAT-NO: 6044428
DOCUMENT-IDENTIFIER: US 6044428 A
** See image for Certificate of Correction **

TITLE: Configurable universal serial bus node

DATE-ISSUED: March 28, 2000

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Rayabhari; Madhu   Cupertino   CA

ASSIGNEE-INFORMATION:
NAME   CITY   STATE ZIP CODE COUNTRY TYPE CODE
Fairchild Semiconductor   South   ME   02
Corporation   Portland

APPL-NO: 09/ 040110   [PALM]
DATE FILED: March 17, 1998

INT-CL: [07] G06 F 13/10, G06 F 13/40, G06 F 15/17, G06 F 3/00

US-CL-ISSUED: 710/129; 710/63, 710/64
US-CL-CURRENT: 710/305; 710/63, 710/64

FIELD-OF-SEARCH: 710/100, 710/101, 710/104, 710/63, 710/64, 710/72, 710/126,
710/129, 710/3, 710/128, 712/37, 345/156, 345/168, 709/231, 370/257, 370/364,
370/912, 455/6.3

PRIOR-ART-DISCLOSED:

                          U.S. PATENT DOCUMENTS

              Search Selected   Search ALL   Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5396639	March 1995	Suenaga et al.	712/37
☐	5485590	January 1996	Hyatt et al.	711/115
☐	5623686	April 1997	Hall et al.	712/32
☐	5659801	August 1997	Kopsaftis	710/62
☐	5784581	July 1998	Hannah	710/110
☐	5818948	October 1998	Gulick	381/77

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☐   5841424   November 1998   Kikinis   345/168
☐   5859993   January 1999   Snyder   712/208
☐   5914877   June 1999   Gulick   364/400.01

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Ishimaru; Mikio

ABSTRACT:

A Universal Serial Bus node having a non-volatile memory is preprogrammed with the
data bits necessary to configure an attached state machine to become a translator
or modified translator for signals from a computer peripheral device. On startup,
the Universal Serial Bus node is configured to translate signals to and from the
computer peripheral device into USB protocol signals to and from a Universal Serial
Bus equipped computer in order to assure proper communication therebetween.

26 Claims, 2 Drawing figures

h   e b   b g e e e f   c   e   c   e   ge

☐ | Generate Collection | | Print |

L4: Entry 12 of 13   File: USPT   Jan 4, 2000

US-PAT-NO: 6012103
DOCUMENT-IDENTIFIER: US 6012103 A

TITLE: Bus interface system and method

DATE-ISSUED: January 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sartore; Ronald H.	San Diego	CA		
Larky; Steven P.	Del Mar	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Cypress Semiconductor Corp.	San Jose	CA			02

APPL-NO: 08/ 886923   [PALM]
DATE FILED: July 2, 1997

INT-CL: [06] G06 F 13/368

US-CL-ISSUED: 710/8; 710/9, 710/10
US-CL-CURRENT: 710/8; 710/10, 710/9

FIELD-OF-SEARCH: 379/395, 709/220, 709/250, 711/114, 711/115, 711/130, 713/100, 710/9

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

| Search Selected | | Search ALL | Clear |

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4641261	February 1987	Dwyer et al.	
☐	4862355	August 1989	Newman et al.	
☐	5289580	February 1994	Latif et al.	
☐	5428748	June 1995	Davidson et al.	710/9
☐	5488657	January 1996	Lynn et al.	379/395
☐	5574859	November 1996	Yeh	
☐	5577213	November 1996	Avery et al.	

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☐	5586268	December 1996	Chen et al.	
☐	5606672	February 1997	Wade	
☐	5615344	March 1997	Corder	
☐	5634074	May 1997	Devon et al.	395/828
☐	5671355	September 1997	Collins	709/250
☐	5687346	November 1997	Shinohara	711/130
☐	5701429	December 1997	Legvold et al.	711/114
☐	5794033	August 1998	Aldebert et al.	713/100
☐	5802558	September 1998	Pierce	711/115
☐	5838907	November 1998	Hansen	709/220

ART-UNIT: 272

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ABSTRACT:

A system and method for reconfiguring a peripheral device connected by a computer
bus and port to a host from a first generic configuration to a second manufacturer
specific configuration is provided in which the configuration of a peripheral
device may be electronically reset. A peripheral interface device for a
standardized computer peripheral device bus and port is also provided in which a
physical disconnection and reconnection of the peripheral device is emulated to
reconfigure the bus and port for a particular peripheral device.

33 Claims, 8 Drawing figures

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